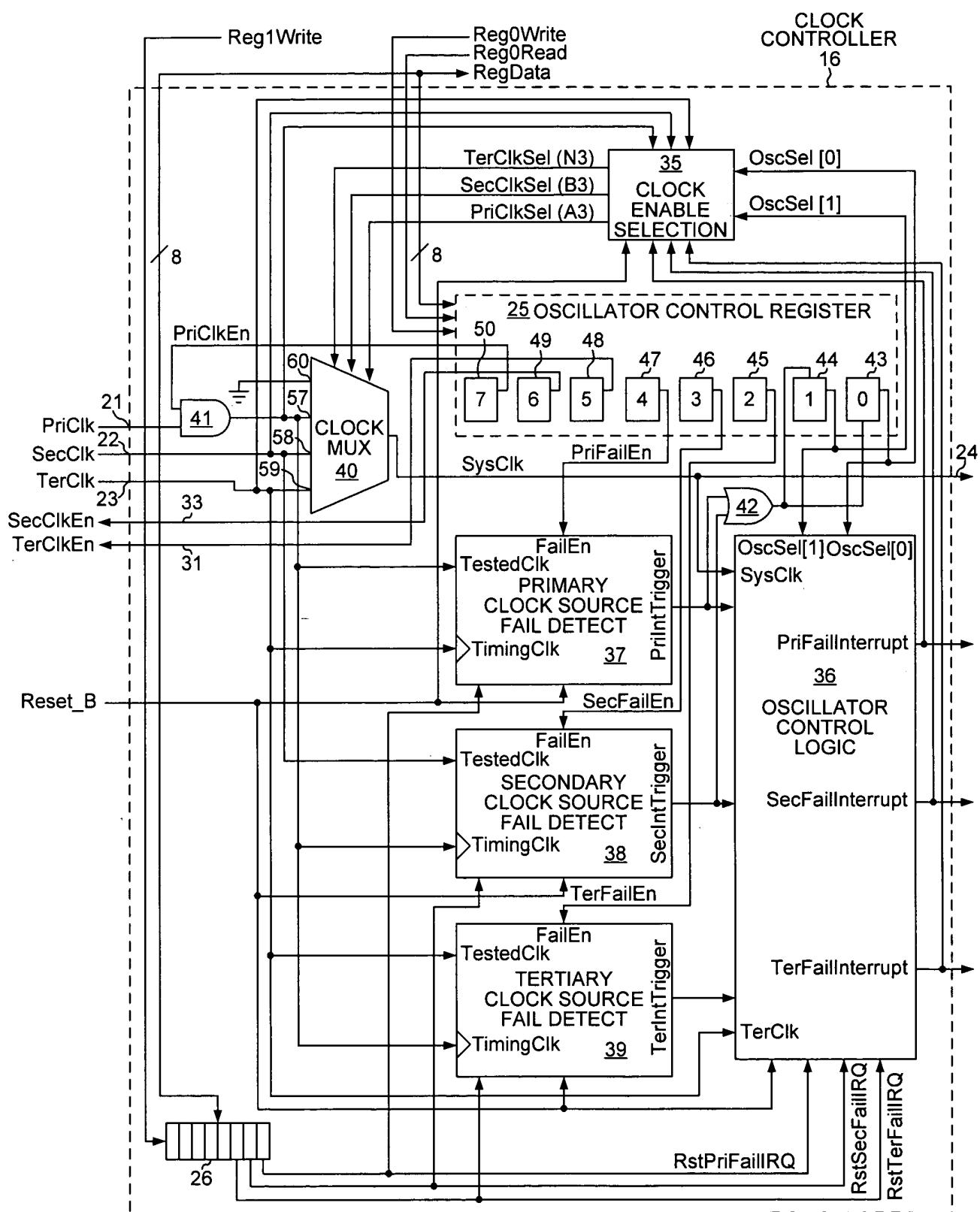
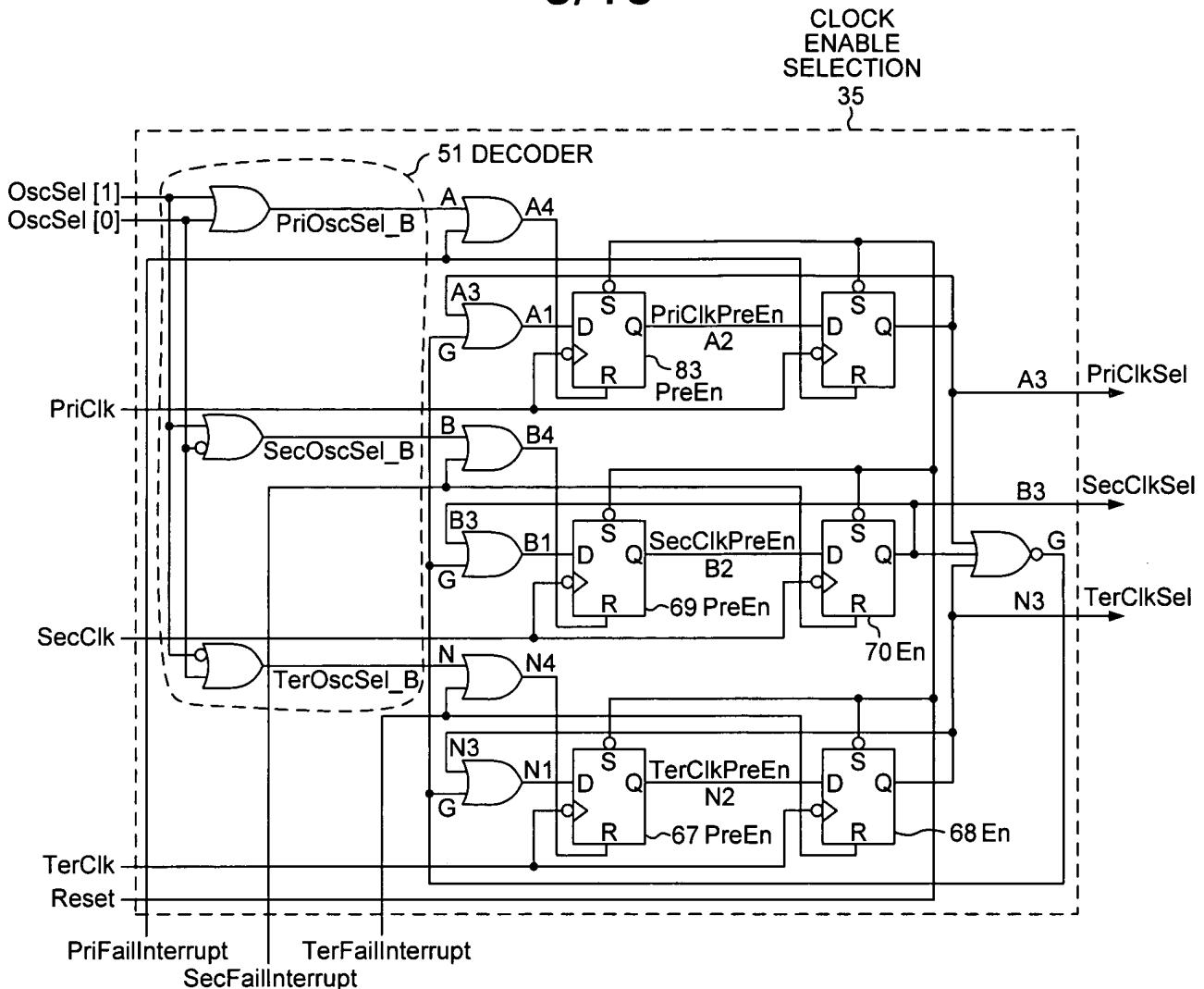


FIG. 1



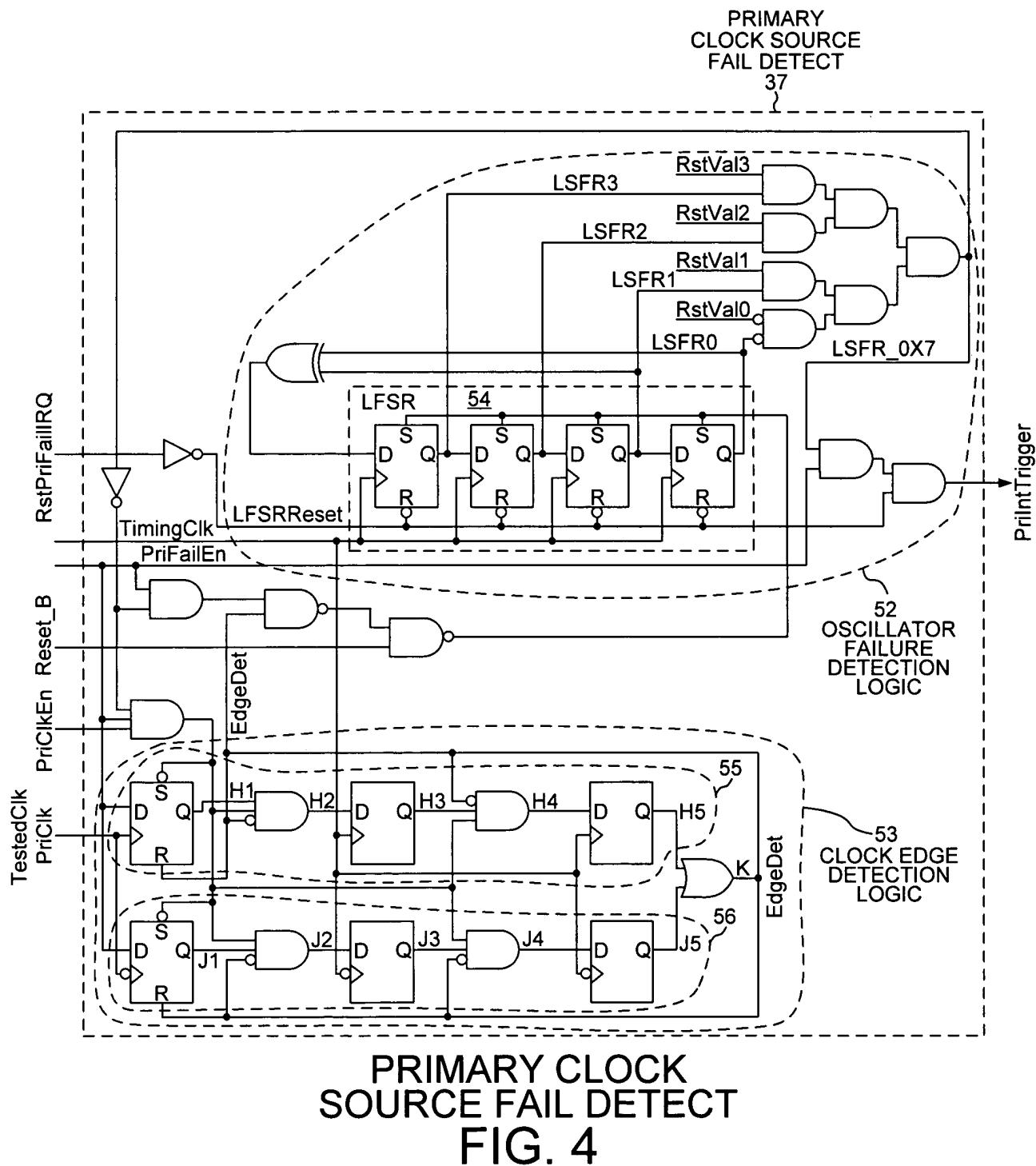
**CLOCK
CONTROLLER
FIG. 2**

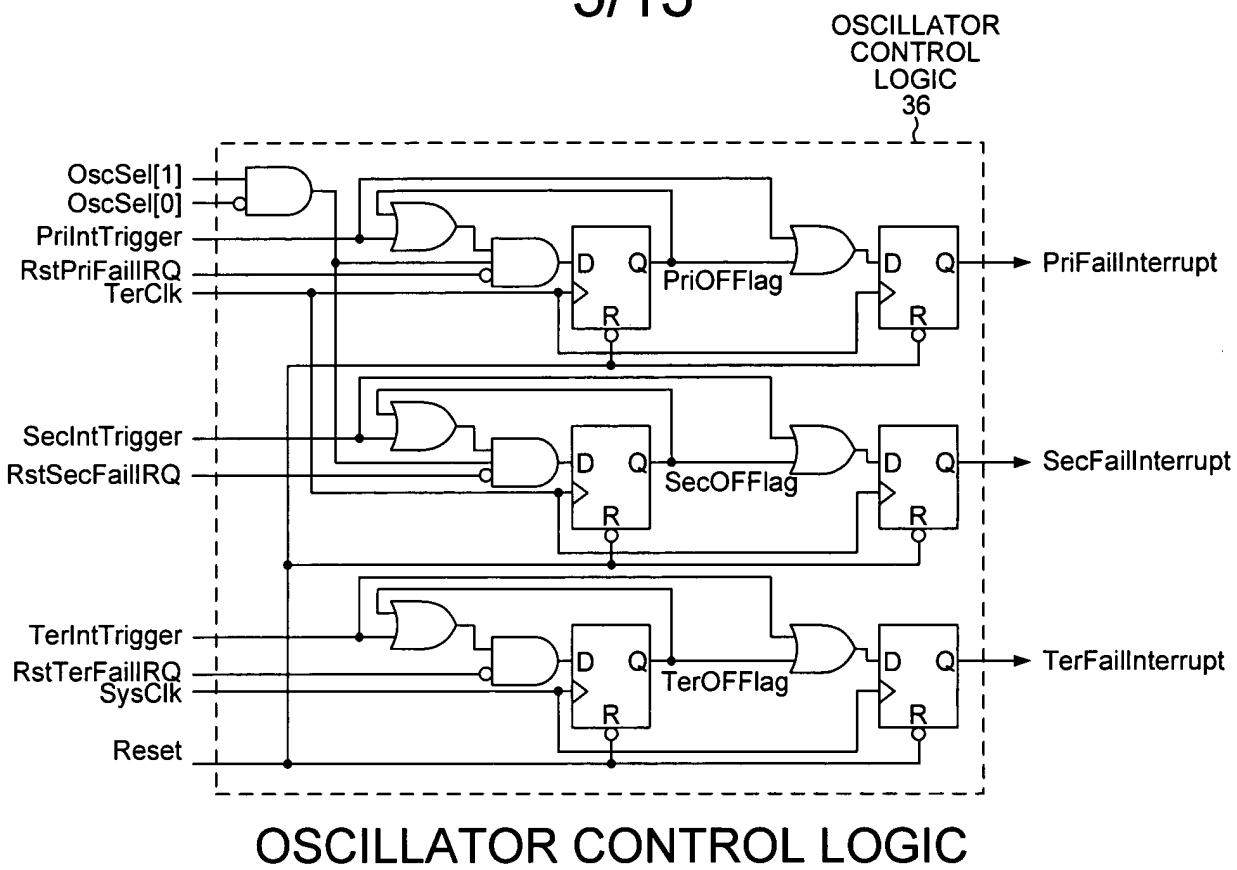


CLOCK ENABLE SELECTION FIG. 3

OUTPUTS FROM CLOCK ENABLE SELECTION 35			INPUTS OF DECODER 51
PriClkSel A3	SecClkSel B3	TerClkSel N3	OscSel [1:0]
1	0	0	00
0	1	0	01
0	0	1	10
0	0	0	11

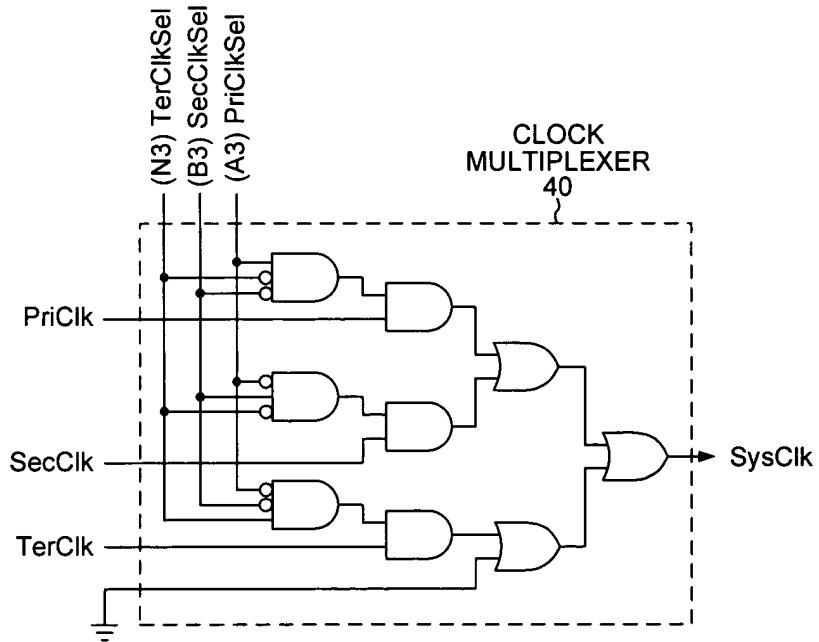
FIG. 7





OSCILLATOR CONTROL LOGIC

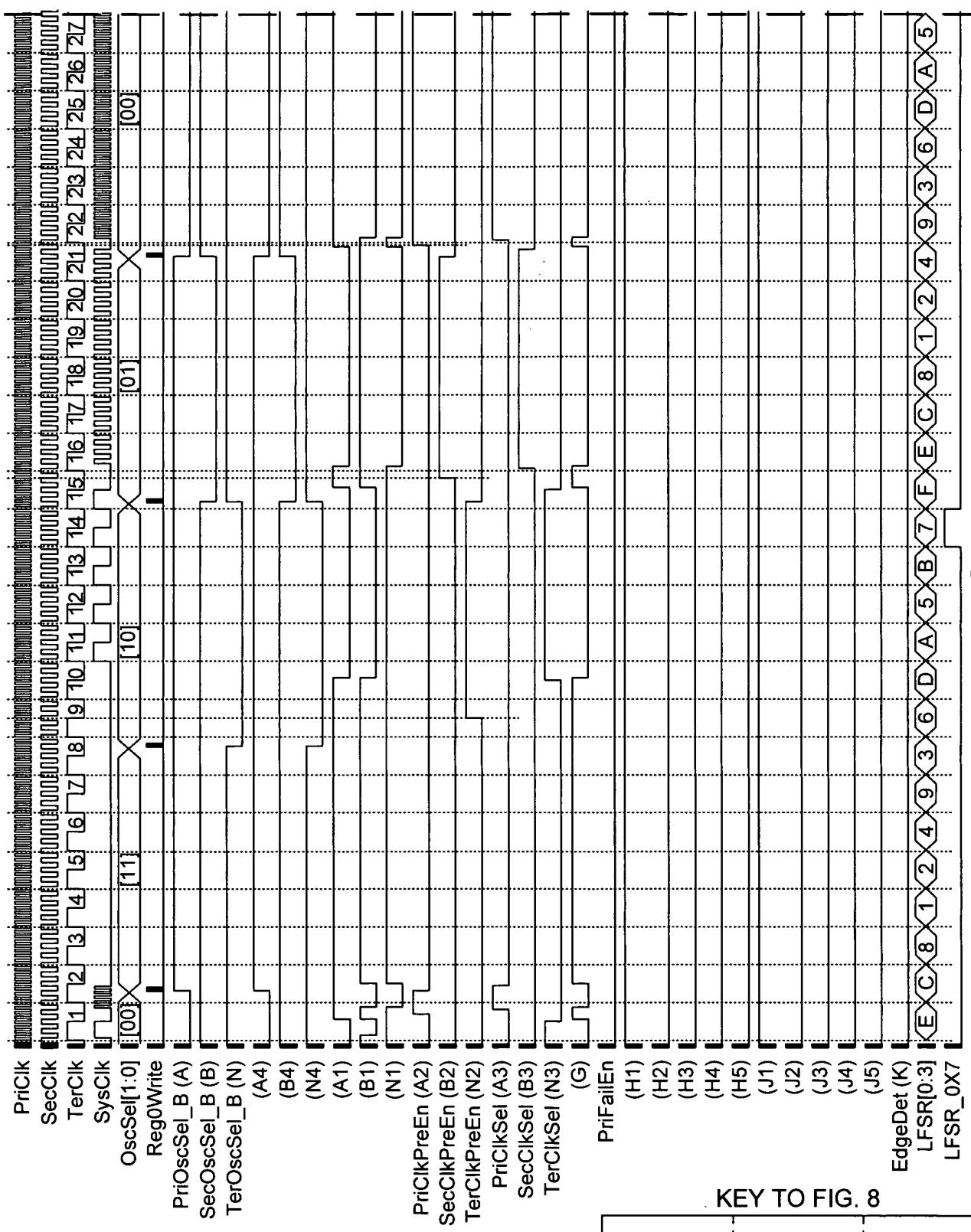
FIG. 5



CLOCK MULTIPLEXER

FIG. 6

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KEY TO FIG. 8

FIG. 8A	FIG. 8B	FIG. 8C
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FIG. 8

FIG. 8A

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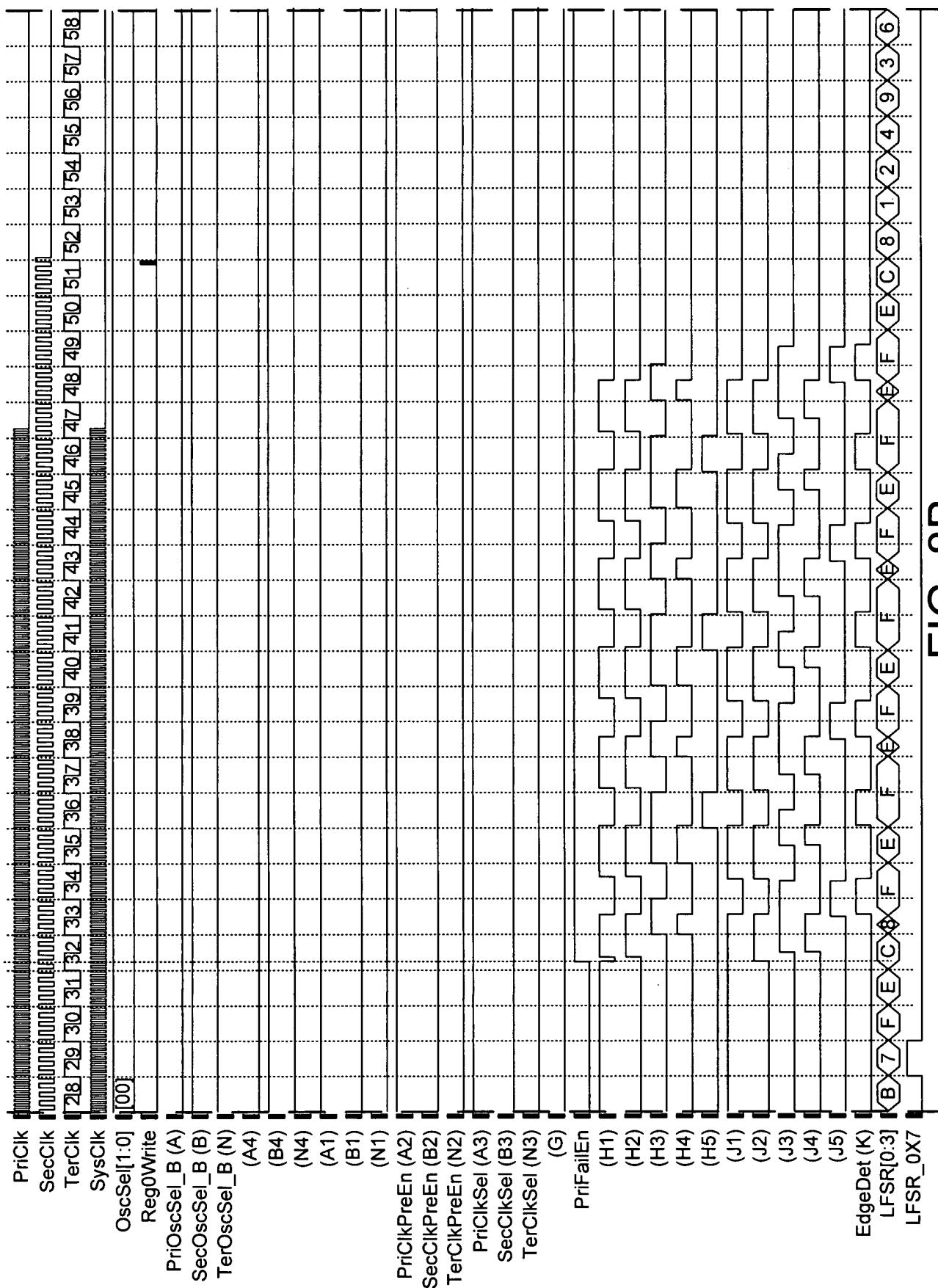


FIG. 8B

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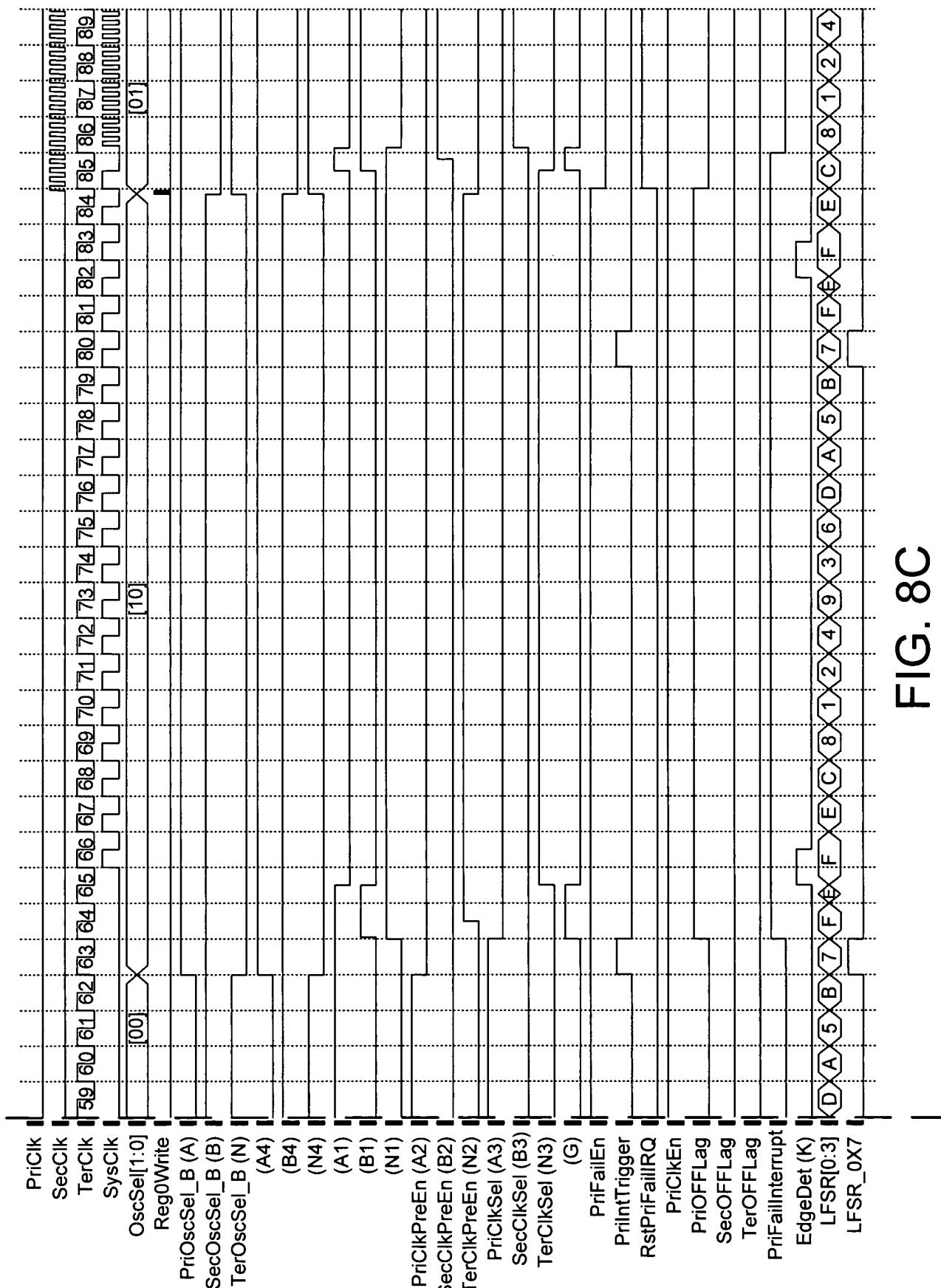
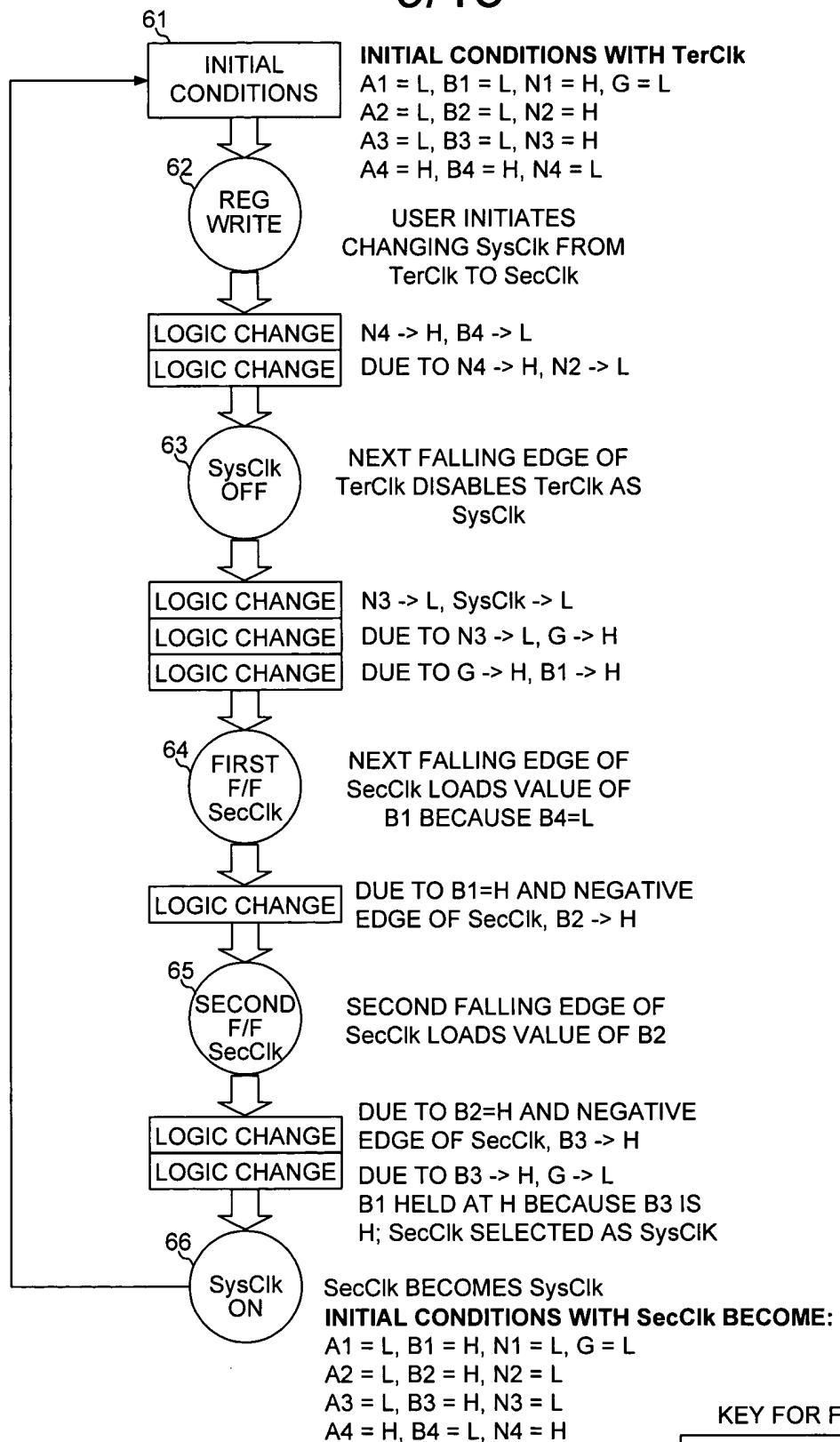


FIG. 8C

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KEY FOR FIGURES 9 - 11

H	MEANS LOGIC HIGH
L	MEANS LOGIC LOW
->	MEANS CHANGES STATE
=	MEANS CURRENT STATE

FIG. 9

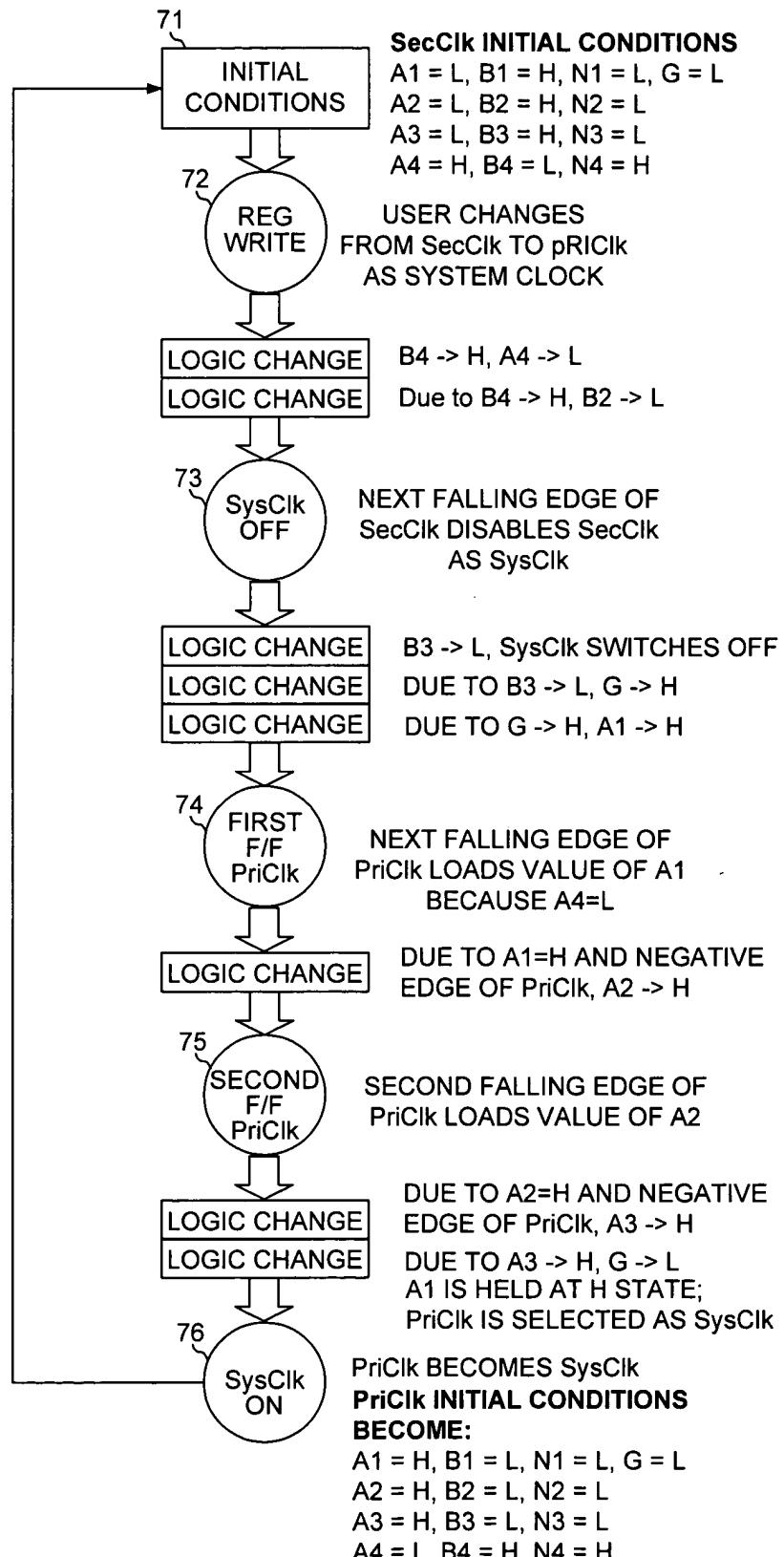


FIG. 10

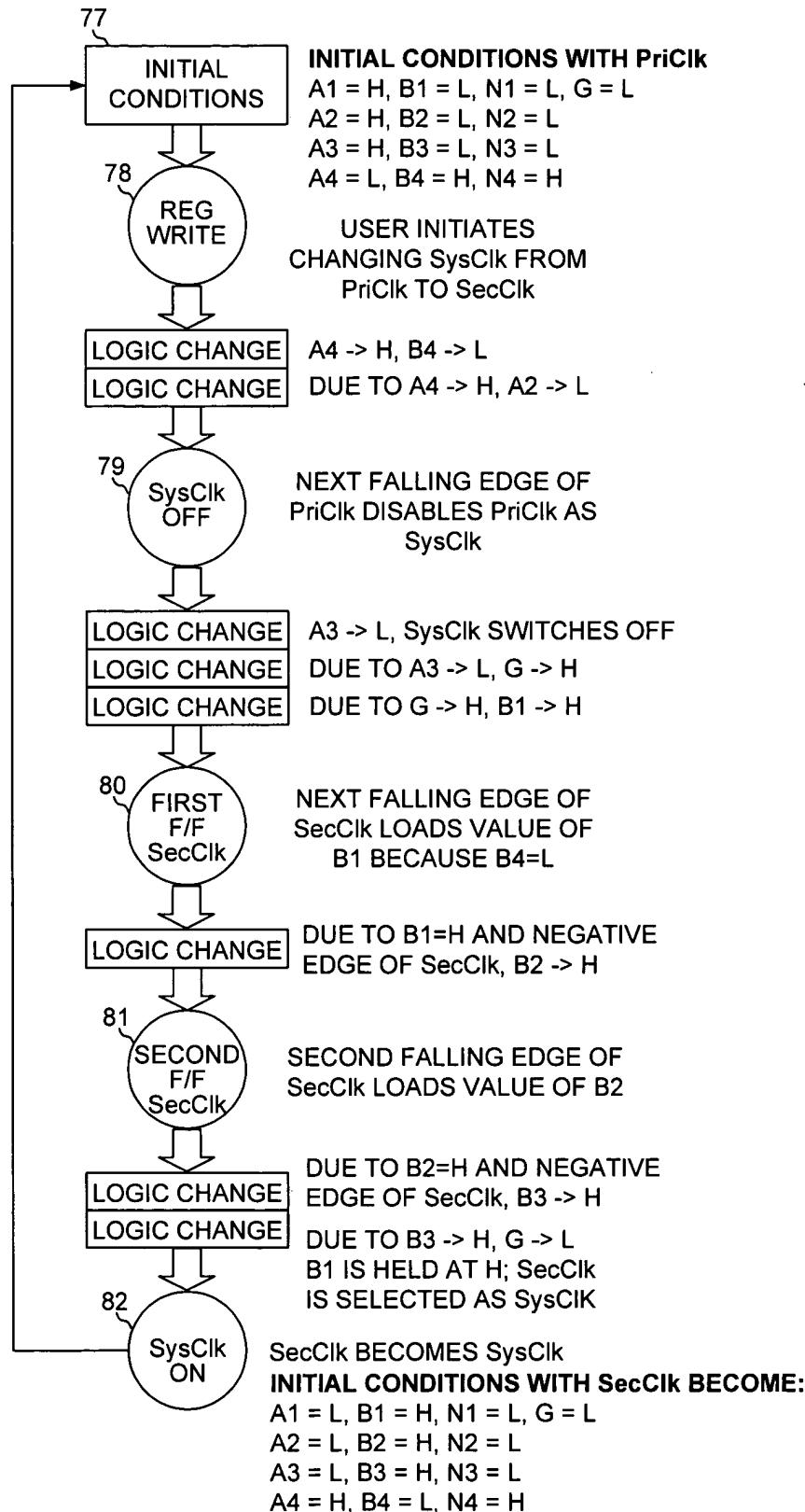
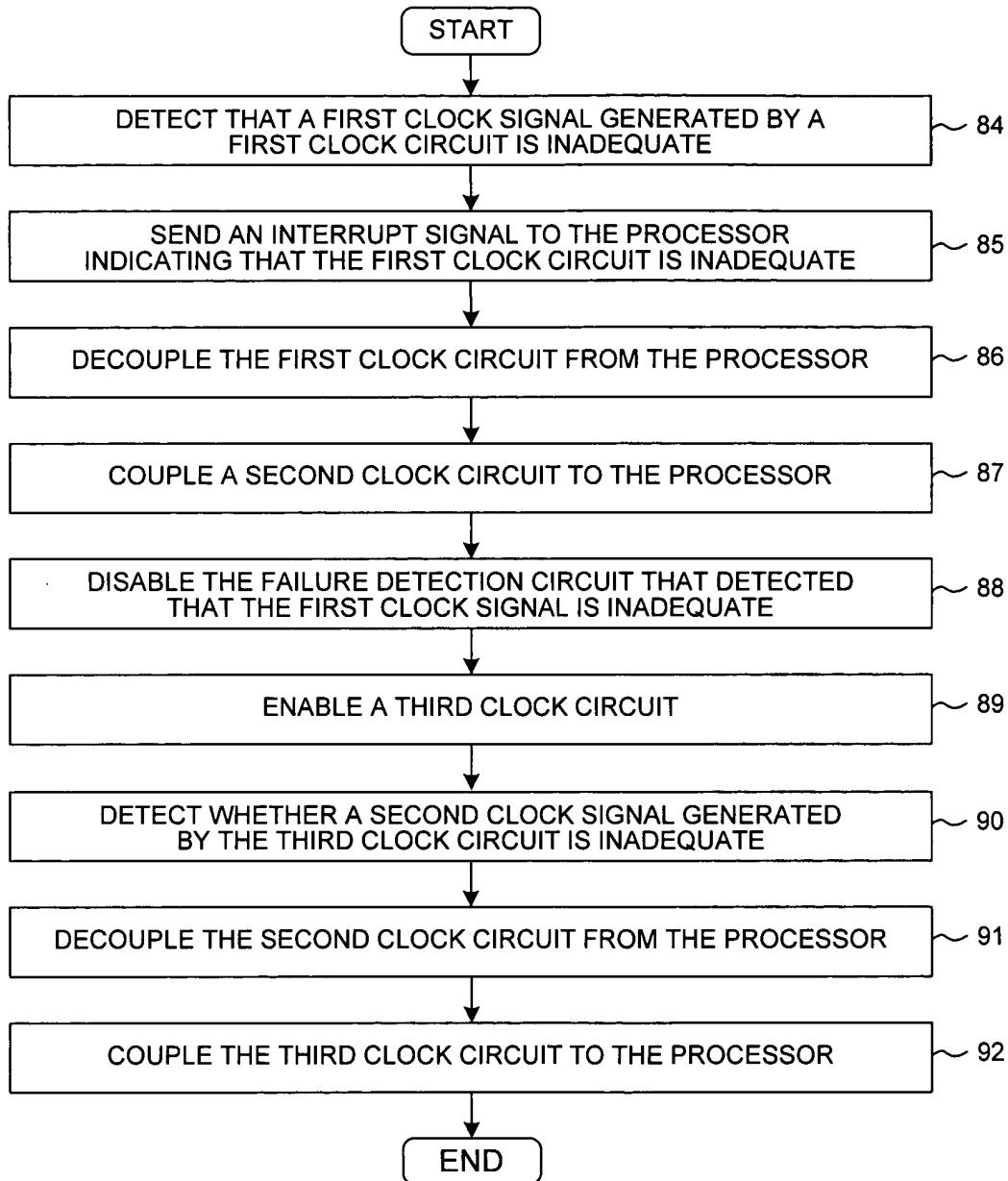


FIG. 11



**SWITCHING FROM A FAILED
CLOCK TO A NEW CLOCK**

FIG. 12

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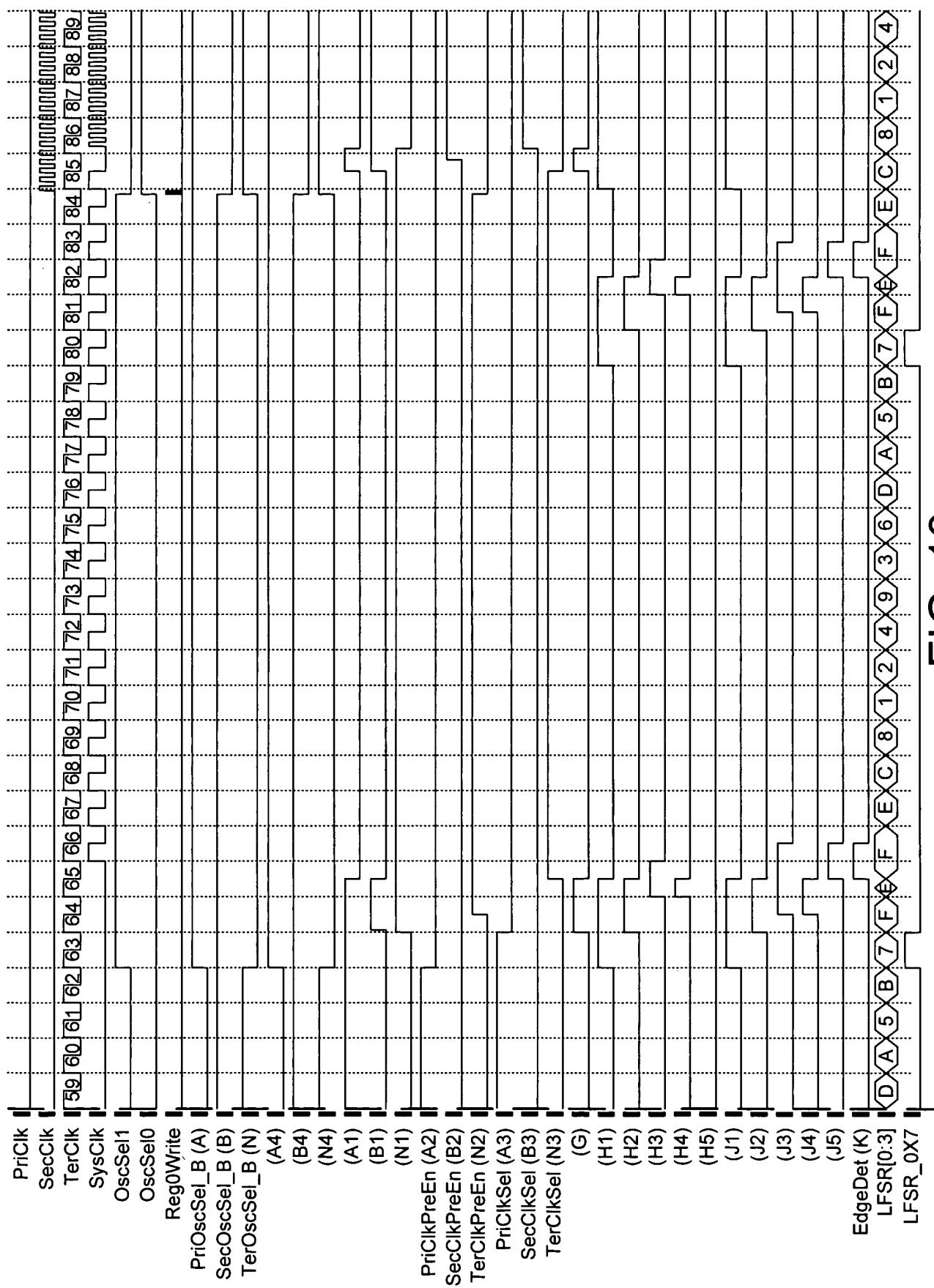


FIG. 13